

### REMARKS

The specification and drawings have been objected to due to informalities. The specification and drawings have been amended appropriately.

Claims 1 and 11 have been rejected under 35 USC 112, second paragraph. Claims 1 and 11 have been amended to conform with 35 USC 112, second paragraph.

Claims 1-3, 6, 9 and 11 have been rejected under 35 USC 102(e) as anticipated by Lai (US Pat. No. 6,763,486); and claims 4, 5, 7, 8 and 10 have been rejected under 35 USC 103(a) as unpatentable over Lai and various combinations of Ichie (US Pat. No. 5,050,187), Phillips (US Pat. No. 3,825,682) and Gotoh (US Pat. App. 2003/0046015). The rejections are respectfully traversed.

Lai is not an appropriate prior art reference under 35 USC 102 since the filing date of Lai (May 9, 2001) is after the priority date (February 28, 2001) of the instant application. Similarly, Gotoh is not an appropriate reference since its filing date (February 26, 2002) is after the priority date (February 28, 2001) of the instant application. A Verified English Translation of the application will be provided upon receipt via supplemental amendment.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing attorney docket no. **449122024500**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

By 

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Attachments

va-85493

### **AMENDMENTS TO THE DRAWINGS**

The attached sheet(s) of drawings includes changes to Figures 1-6.

Attachment:      Replacement sheet  
                         Annotated sheet showing changes



**REPLACEMENT SHEET**

FIG 1

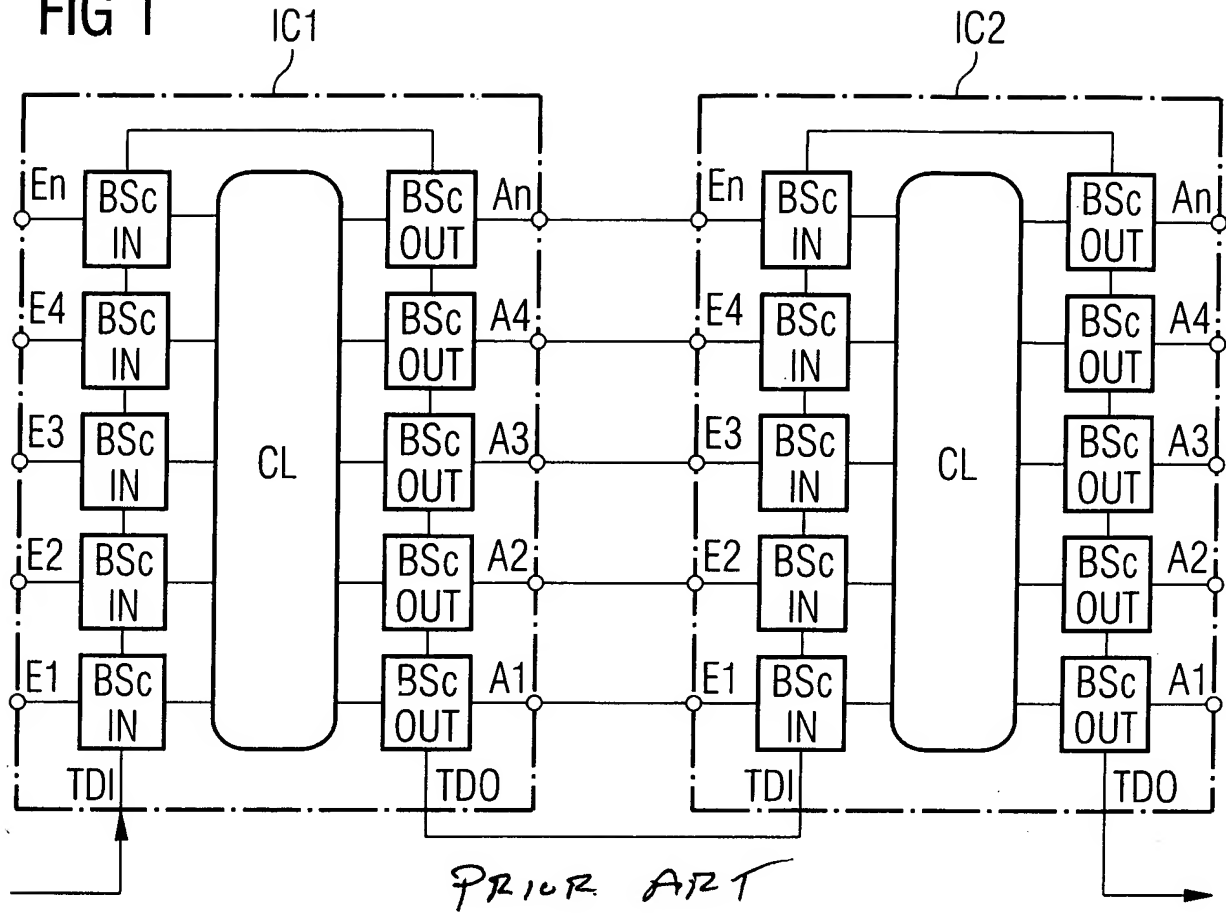
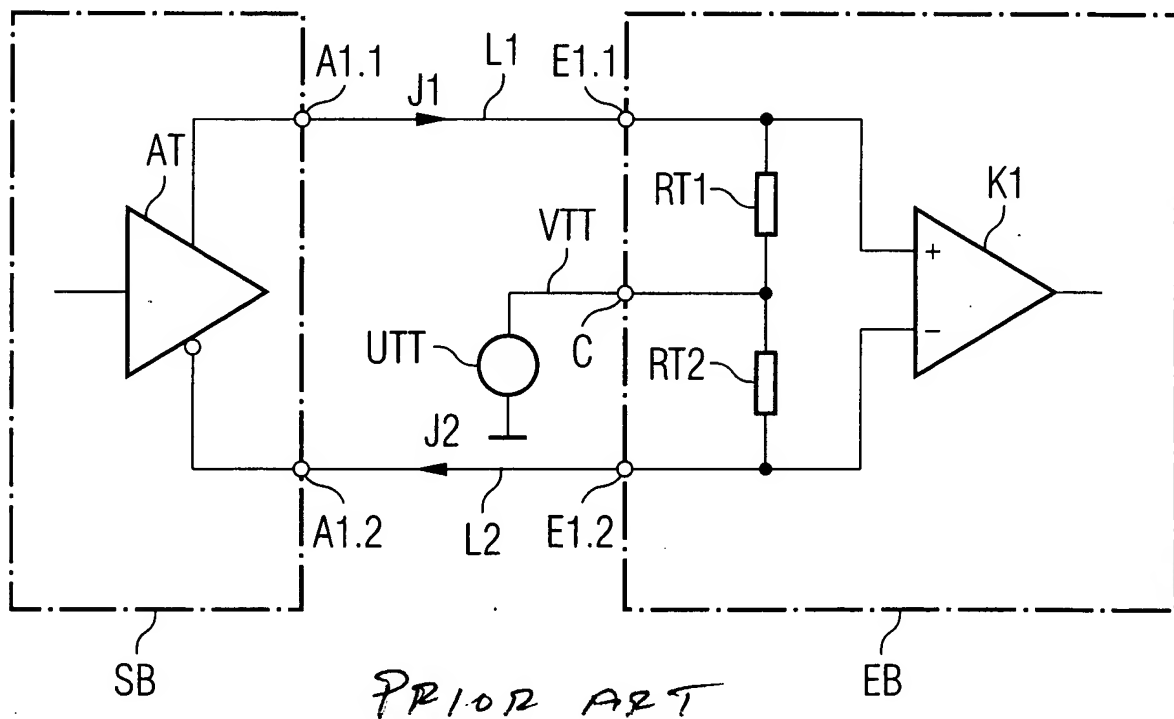


FIG 2



ANNOTATED

FIG 3

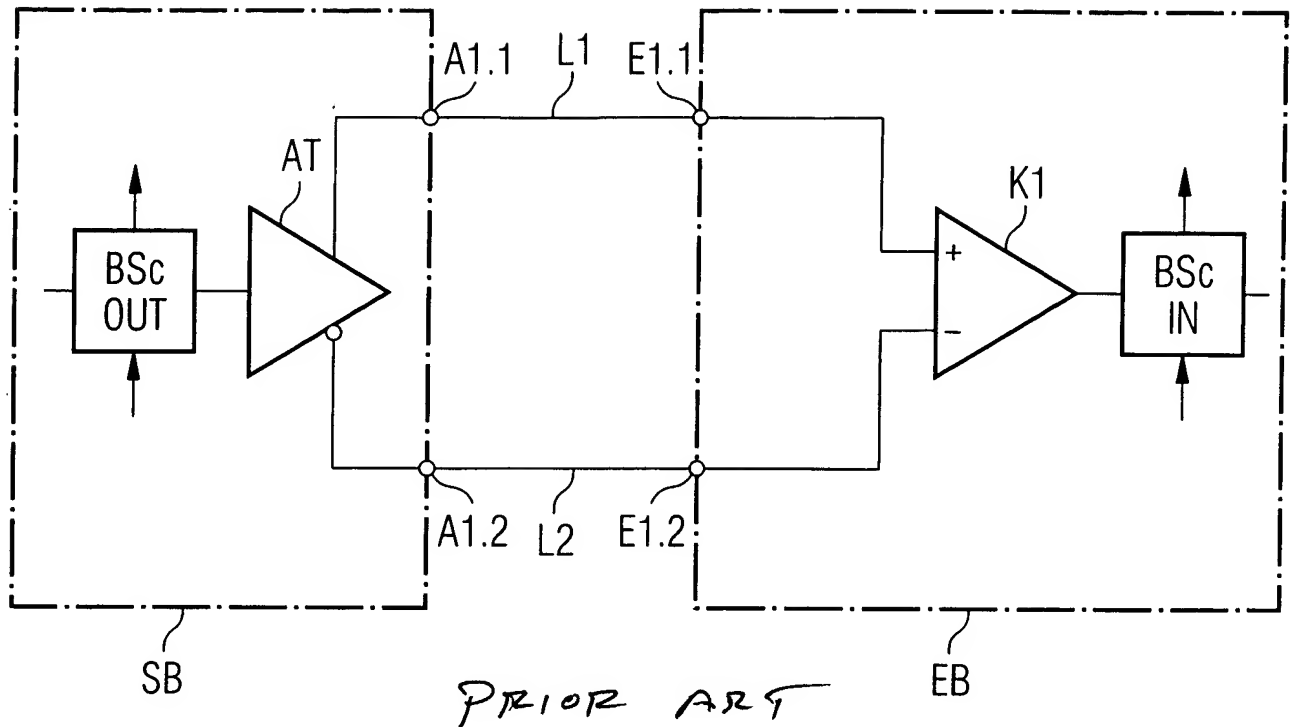
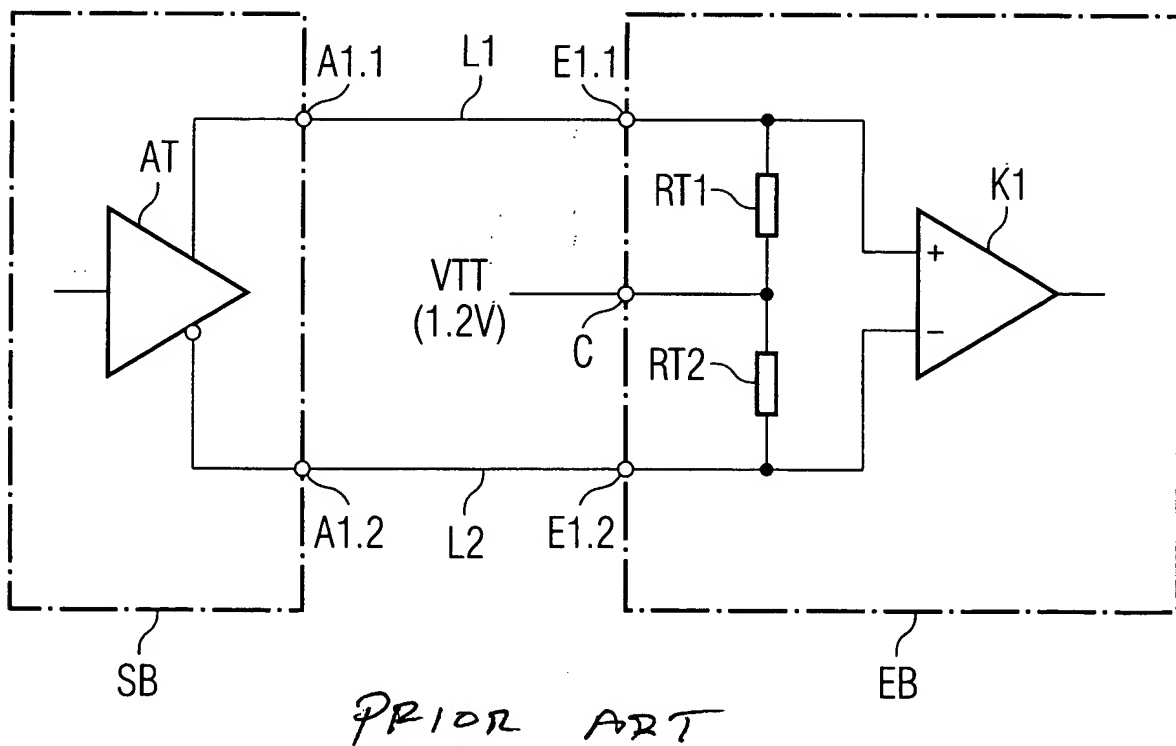


FIG 4



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The diagram illustrates a prior art differential amplifier circuit, divided into two main sections: CML AT (Current Mode Logic At) and EB (Euler Block). The CML AT section contains three MOSFETs: M1, M2, and M3. M1 and M2 are connected in a differential pair configuration, with their sources tied together and connected to ground through M3. The gates of M1 and M2 are connected to a common input signal. The drains of M1 and M2 are connected to a common output node. The EB section contains a differential amplifier K1, which is connected to the output node of the CML AT section. The differential amplifier K1 has two inputs, labeled + and -, and a single output. The circuit is powered by a supply voltage VTT. The output of the differential amplifier K1 is connected to a load resistor RT1. The circuit is labeled with various components and nodes: M1, M2, M3, CML AT, EB, VTT, RT1, RT2, K1, A1.1, L1, E1.1, A1.2, L2, E1.2, and SB.